REMARKS

I. Allowed and Allowable Claims

Applicants appreciate the Examiner's allowance of Claims 1-7 and 17-29 and the indication of allowability of dependent Claims 9, 10, 12-16, and 31-34. In this Amendment, Applicants have re-written dependent Claims 31-34 in independent form. In accordance with the Examiner's indication of allowability, Applicants respectfully submit that Claims 31-34 are now in condition for allowance.

II. Amendments to the Specification

Applicants have amended the specification to insert serial numbers and filing dates for applications formerly identified by attorney docket number.

III. 35 U.S.C. § 102(b) Rejections

Independent Claims 8 and 30 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,878,203 to Matsumoto et al. Applicants respectfully request reconsideration and withdrawal of those rejections in view of the amendments and remarks made herein.

A. Independent Claim 8

Independent Claim 8 recites storing a plurality of bits in a register in a first direction and reading the plurality of bits from the register in a second direction. In the Office Action, it was asserted that Matsumoto et al. teaches these elements because Matsumoto et al. describes moving bits from a host to a buffer (the purported "first direction") and then moving the bits from the buffer to a disk array (the purported "second direction"). In other words, the first direction was asserted to correspond to input to the buffer, and the second direction was asserted to correspond to output from the buffer.

In response to this rejection, Applicants have amended independent Claim 8 to clarify that first and second directions do not refer to input and output to and from the buffer but to the internal storage and reading of bits within the buffer. Specifically, independent Claim 8 now recites that an order in which the plurality of bits are read from the register is different from an order in which the plurality of bits are stored in the register, whereby bits that are adjacent to one another when provided to the memory device are not adjacent to one another when read from the register. Matsumoto et al. does not teach this element. In Matsumoto et al., the bits are read and stored in the buffer in the same order. Accordingly, bits that are adjacent to one another when provided from the host to the buffer are adjacent to one another when read from the buffer.

In view of the amendment to Claim 8, Applicants respectfully submit that the rejection of Claim 8 should be withdrawn.

B. Independent Claim 30

Independent Claim 30 recites, with a host device, providing a plurality of bits to a memory device such that the memory device will store adjacent bits of the plurality of bits in non-adjacent storage locations in a memory array. In the Office Action, it was asserted that Matsumoto et al. teaches this act because a RAID 3/5 system scatters bits across different disk drives. To clarify the invention, Applicants have amended Claim 30 to recite functionality not taught in Matsumoto et al. Specifically, amended Claim 30 now recites that the host device re-orders a plurality of bits such that bits that are adjacent to one another before the re-ordering are not adjacent to one another after the re-ordering. The host device provides the re-ordered plurality of bits to the memory device, and the memory device stores the re-ordered plurality of bits in the memory array in the same order as provided to the memory device by the host device.

This functionality is not taught in Matsumoto et al. As a first matter, the component that performs the RAID 3/5 scattering in Matsumoto et al. is the array controller 13, and that component is in the memory device — not the host device (the host computer 1). Accordingly, to the extent that the RAID 3/5 scattering in Matsumoto et al. is "re-ordering" of bits, Matsumoto et al. teaches that that functionality is performed by the memory device — not the host device, as recited in amended Claim 30. Also, because the array controller 13 performs RAID 3/5 scattering, it does not not store bits in the same order as provided to the memory device by the host device, as recited in amended Claim 30.

In view of the amendment to Claim 30, Applicants respectfully submit that the rejection of Claim 30 should be withdrawn.

IV. Conclusion

In view of the above amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Reconsideration is respectfully requested. If there are any questions concerning this Amendment, the Examiner is invited to contact the undersigned attorney at (312) 321-4719.

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Respectfully submitted,

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